

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
RELEASE 1.4Welcome
United States Patent and Trademark Office[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#) [Quick Links](#)

» Search

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents


- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

 Print Format

Your search matched **30** of **945745** documents.
Results are shown **15** to a page, sorted by **publication year** in **descending** order.

Results:Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 Yield modeling of a WSI telecom router architecture**

Bing Qiu; Savaria, Y.; Meng Lu; Chunyan Wang; Thibeault, C.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17
International Symposium on , 6-8 Nov. 2002
Page(s): 314 -321

[\[Abstract\]](#) [\[PDF Full-Text \(270 KB\)\]](#) **IEEE CNF****2 Speeding-up I/sub DDQ/ measurements**

Thibeault, C.;
VLSI Test Symposium, 2002. (VTS 2002). Proceedings 20th IEEE , 28 April-2
Page(s): 295 -301

[\[Abstract\]](#) [\[PDF Full-Text \(284 KB\)\]](#) **IEEE CNF****3 An efficient FPGA implementation of a pulse-shaping IIR filter**

Batani, N.; Thibeault, C.; Gargour, C.S.;
Electrical and Computer Engineering, 2001. Canadian Conference on , Volume
13-16 May 2001
Page(s): 353 -355 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) **IEEE CNF****4 Tools for the characterization of bipolar CML testability**

Monte, G.; Antaki, B.; Patenaude, S.; Savaria, Y.; Thibeault, C.; Trouborst, P.
VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001 , 29 April-3 May
Page(s): 388 -395

[\[Abstract\]](#) [\[PDF Full-Text \(632 KB\)\]](#) **IEEE CNF****5 Improving Delta-I_{DDQ}-based test methods**

Thibeault, C.;
Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000
Page(s): 207 -216

[\[Abstract\]](#) [\[PDF Full-Text \(692 KB\)\]](#) **IEEE CNF**

6 Efficient diagnosis of single/double bridging faults with Delta Iddq probabilistic signatures and Viterbi algorithm

Thibeault, C.;

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000

Page(s): 431 -438

[\[Abstract\]](#) [\[PDF Full-Text \(56 KB\)\]](#) **IEEE CNF**

7 On the adaptation of Viterbi algorithm for diagnosis of multiple bridging faults

Thibeault, C.;

Computers, IEEE Transactions on , Volume: 49 Issue: 6 , June 2000

Page(s): 575 -587

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) **IEEE JNL**

8 An histogram based procedure for current testing of active defects

Thibeault, C.;

Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999

Page(s): 714 -723

[\[Abstract\]](#) [\[PDF Full-Text \(804 KB\)\]](#) **IEEE CNF**

9 On the comparison of ΔI_{DDQ} and I_{DDQ} testing

Thibeault, C.;

VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 25-29 April 1999

Page(s): 143 -150

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) **IEEE CNF**

10 A scan-based configurable, programmable, and scalable architecture for sliding window-based operations

Thibeault, C.; Begin, G.;

Computers, IEEE Transactions on , Volume: 48 Issue: 6 , June 1999

Page(s): 615 -627

[\[Abstract\]](#) [\[PDF Full-Text \(748 KB\)\]](#) **IEEE JNL**

11 Can the current behavior of faulty and fault-free ICs and the impact on diagnosis

Thibeault, C.; Boisvert, L.;

Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on , 2-4 Nov. 1998

Page(s): 202 -210

[\[Abstract\]](#) [\[PDF Full-Text \(36 KB\)\]](#) **IEEE CNF**

12 Increasing current testing resolution

Thibeault, C.;

Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on , 2-4 Nov. 1998

Page(s): 126 -134

[\[Abstract\]](#) [\[PDF Full-Text \(44 KB\)\]](#) **IEEE CNF**

13 Diagnosis method based on ΔI_{ddq} probabilistic signatures: experimental results

Thibeault, C.; Boisvert, L.;

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998

Page(s): 1019 -1026

[\[Abstract\]](#) [\[PDF Full-Text \(592 KB\)\]](#) **IEEE CNF**

14 VLSI implementation of a high speed second order sigma-delta mo with high-performance integrators

Hosseinzadeh, E.; Belzile, J.; Thibeault, C.;

Electrical and Computer Engineering, 1998. IEEE Canadian Conference on , Vo 24-28 May 1998

Page(s): 545 -548 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) **IEEE CNF**

15 A novel probabilistic approach for IC diagnosis based on differential quiescent current signatures

Thibeault, C.;

VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997

Page(s): 80 -85

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) **IEEE CNF**

1 2 [\[Next\]](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved

[IEEE HOME](#) | [SEARCH IEEE](#) | [SHOP](#) | [WEB ACCOUNT](#) | [CONTACT IEEE](#)[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)**IEEE Xplore**
RELEASE 1.4Welcome
United States Patent and Trademark Of[Help](#) [FAQ](#) [Terms](#) [IEEE Peer](#) [Quick Links](#) [Review](#)[» Search](#)**Welcome to IEEE Xplore***

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

 [Print Format](#)Your search matched **30** of **945745** documents.Results are shown **15** to a page, sorted by **publication year** in **descending** order.**Results:**Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****16 Are defect-tolerant circuits with redundancy really cost-effective? C and realistic cost model***Gagnon, Y.; Savaria, Y.; Meunier, M.; Thibeault, C.;*

Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE International Symposium on , 20-22 Oct. 1997

Page(s): 157 -165

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#) **IEEE CNF****17 A cost model for VLSI/MCM systems***Kafrouni, M.; Thibeault, C.; Savaria, Y.;*

Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE International Symposium on , 20-22 Oct. 1997

Page(s): 148 -156

[\[Abstract\]](#) [\[PDF Full-Text \(356 KB\)\]](#) **IEEE CNF****18 Experimental results from I_{DDF} testing***Thibeault, C.; Payeur, A.;*

Defect and Fault Tolerance in VLSI Systems, 1996. Proceedings., 1996 IEEE International Symposium on , 6-8 Nov. 1996

Page(s): 185 -193

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) **IEEE CNF****19 Detection and location of faults and defects using digital signal pro***Thibeault, C.;*

VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995

Page(s): 262 -267

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) **IEEE CNF****20 M-path decoder with algebraic metric calculation***Alie, M.; Belzile, J.; Thibeault, C.;*

Electrical and Computer Engineering, 1995. Canadian Conference on , Volume

Sept. 1995
Page(s): 225 -228 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) [IEEE CNF](#)

21 FFT-based test of a yield monitor circuit

Thibeault, C.; Payeur, A.;

Defect and Fault Tolerance in VLSI Systems, 1995. Proceedings., 1995 IEEE International Workshop on , 13-15 Nov. 1995

Page(s): 243 -251

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) [IEEE CNF](#)

22 Equivalence proofs of some yield modeling methods for defect-tolerant integrated circuits

Thibeault, C.; Savaria, Y.; Houle, J.L.;

Computers, IEEE Transactions on , Volume: 44 Issue: 5 , May 1995

Page(s): 724 -728

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) [IEEE JNL](#)

23 Using Fourier analyses to enhance IC testability

Thibeault, C.;

Defect and Fault Tolerance in VLSI Systems, 1994. Proceedings., The IEEE International Workshop on , 17-19 Oct. 1994

Page(s): 280 -288

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) [IEEE CNF](#)

24 Using sinusoidal stimuli and Fourier analyses for memory IC testing

Thibeault, C.;

Memory Technology, Design and Testing, 1994., Records of the IEEE International Workshop on , 8-9 Aug. 1994

Page(s): 92 -97

[\[Abstract\]](#) [\[PDF Full-Text \(400 KB\)\]](#) [IEEE CNF](#)

25 A connectivity based, table-driven decoder for convolutional codes

Begin, G.; Thibeault, C.;

Information Theory, 1994. Proceedings., 1994 IEEE International Symposium June-1 July 1994

Page(s): 166

[\[Abstract\]](#) [\[PDF Full-Text \(72 KB\)\]](#) [IEEE CNF](#)

26 A fast method to evaluate the optimum number of spares in defect-tolerant integrated circuits

Thibeault, C.; Savaria, Y.; Houle, J.-L.;

Computers, IEEE Transactions on , Volume: 43 Issue: 6 , June 1994

Page(s): 687 -697

[\[Abstract\]](#) [\[PDF Full-Text \(948 KB\)\]](#) **IEEE JNL**

27 Some results on yield and local design rule relaxation

Crepeau, J.; Thibeault, C.; Savaria, Y.;

Defect and Fault Tolerance in VLSI Systems, 1993., The IEEE International Workshop on , 27-29 Oct. 1993

Page(s): 144 -151

[\[Abstract\]](#) [\[PDF Full-Text \(292 KB\)\]](#) **IEEE CNF**

28 An inexpensive method of detecting localised parametric defects in RAM

Savaria, Y.; Thibeault, C.;

Memory Testing, 1993., Records of the 1993 IEEE International Workshop on Aug. 1993

Page(s): 90 -95

[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) **IEEE CNF**

29 Comparing results from defect-tolerant yield models

Thibeault, C.; Savaria, Y.;

Defect and Fault Tolerance in VLSI Systems, 1992. Proceedings., 1992 IEEE International Workshop on , 4-6 Nov. 1992

Page(s): 22 -31

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) **IEEE CNF**

30 Impact of reconfiguration logic on the optimization of defect-tolerant integrated circuits

Thibeault, C.; Houle, J.L.;

Fault-Tolerant Computing, 1990. FTCS-20. Digest of Papers., 20th International Symposium , 26-28 June 1990

Page(s): 158 -165

[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) **IEEE CNF**

[\[Prev\]](#) [1](#) [2](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved